

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L8	716	(PLL or (phase adj locked adj loop)) and (integer with (divider or synthesizer)) and (fractional with (divider or synthesizer))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:46
L9	555	(PLL or (phase adj locked adj loop)) and (integer with (divider or synthesizer)) same (fractional with (divider or synthesizer))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 13:37
L10	496	(PLL or (phase adj locked adj loop)) and (integer with (divider or synthesizer)) with (fractional with (divider or synthesizer))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 13:37
L11	496	((PLL or (phase adj locked adj loop))) and ((integer with (divider or synthesizer)) with (fractional with (divider or synthesizer)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 13:39
L12	42	(second adj (PLL or (phase adj locked adj loop))) and ((integer with (divider or synthesizer)) with (fractional with (divider or synthesizer)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 13:39
L17	3	transmit with receive with (two adj dipole adj antenna)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 18:17
L18	16	transmit\$4 with receiv\$3 with (two adj dipole adj antenna)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 18:17

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L19	5	(first adj ((phase adj locked adj loop) or pll)) with ((second adj ((phase adj locked adj loop) or pll)) with (VCO or (voltage adj controlled adj oscillator))) and mobile adj station	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 18:10
L20	155	transmit\$4 with receiv\$3 and (two adj dipole adj antenna)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 18:17
L21	5	transmit\$4 with receiv\$3 and (two adj dipole adj antenna) and pll	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 18:18
L22	5	transmit\$4 same receiv\$3 and (two adj dipole adj antenna) and pll	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 18:18
L23	5	transmit\$4 and receiv\$3 and (two adj dipole adj antenna) and pll	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 18:18
L24	178	transmit\$4 and receiv\$3 and (two adj dipole adj antenna)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 18:19
L25	89	transmit\$4 and receiv\$3 and (two with dipole with antenna) and pll	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 18:19

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L26	88	transmit\$4 same receiv\$3 and (two with dipole with antenna) and pll	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 18:19
L27	88	transmit\$4 with receiv\$3 and (two with dipole with antenna) and pll	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 18:19
L28	7	("5107335" "5423085" "5432855" "5436927" "5633898" "5727030" "5768321").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/01/23 19:37
L29	67331	internal and antenna	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 19:42
L30	2879	internal adj antenna	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 19:42
L31	4	internal adj antenna and transceiver	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 19:42
L32	887	internal adj antenna and transceiver	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 19:43

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L33	131	internal adj antenna with transceiver	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 19:43
L34	3	internal adj antenna with transceiver and pll	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:03
L35	5	internal adj antenna same transceiver and pll	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 19:44
L36	20	internal adj antenna and transceiver and pll	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 19:44
L37	1	WO99/08456	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 19:53
L38	107	"08456"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 19:53
L39	2	"99/08456"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 19:53

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L40	5	"9908456"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 19:53
L41	2	internal adj antenna with TDMA	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:05
L42	8	internal adj antenna same TDMA	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:09
L43	195	internal adj antenna and TDMA	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:09
L44	4460	375/376	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:45
L45	155	8 and 44	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:46
L46	1	"10/396118"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:46

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L47	89	(first adj ((phase adj locked adj loop) or pll)) with ((second adj ((phase adj locked adj loop) or pll)) with (VCO or (voltage adj controlled adj oscillator))) and ((mobile adj station) or MS or (base adj station))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:46
L48	184	(first adj ((phase adj locked adj loop) or pll)) with ((second adj ((phase adj locked adj loop) or pll)) with (VCO or (voltage adj controlled adj oscillator)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:46
L49	62	(first adj synthesizer) and (second adj synthesizer) and ((phase adj locked adj loop) or pll)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:46
L50	1	"10/664850"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:46
L51	2	"6,489,818".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:46
L52	0	"10664850"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:46
L53	282	(first adj ((phase adj locked adj loop) or pll)) same ((second adj ((phase adj locked adj loop) or pll)) with (VCO or (voltage adj controlled adj oscillator)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:50

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L54	381	(first adj ((phase adj locked adj loop) or pll)) and ((second adj ((phase adj locked adj loop) or pll)) with (VCO or (voltage adj controlled adj oscillator)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:46
L55	1636	(first adj ((phase adj locked adj loop) or pll)) and (second adj ((phase adj locked adj loop) or pll))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:46
L56	89	(first adj ((phase adj locked adj loop) or pll)) with ((second adj ((phase adj locked adj loop) or pll)) with (VCO or (voltage adj controlled adj oscillator))) and ((mobile adj station) or MS or (base adj station) or CDMA or wlan)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:46
L57	418	peregrine	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:46
L58	12	peregrine and pll	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:46
L59	184	(first adj ((phase adj locked adj loop) or pll)) with ((second adj ((phase adj locked adj loop) or pll)) with (VCO or (voltage adj controlled adj oscillator)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:46
L60	10	("5038115" "5072195" "5302919" "5374904" "5382922" "5414390" "5559473" "5579184" "5657359" "5734301").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/01/23 20:46

EAST Search History

L61	2	"5838730".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:46
L62	3	"7003686".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:46
L63	2	"4720688".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:46
L64	1	(first adj ((phase adj locked adj loop) or pll)) with ((second adj ((phase adj locked adj loop) or pll)) with (VCO or (voltage adj controlled adj oscillator))) and (wlan)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:46
L65	2	pe3291	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:46
L66	0	peredrine	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:46
L67	0	pe3292	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:46

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L68	2	(first adj ((phase adj locked adj loop) or pll)) and ((second adj ((phase adj locked adj loop) or pll)) and (VCO or (voltage adj controlled adj oscillator))) and (wlan)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:46
L69	2	"6090648".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:46
L70	0	(first adj ((phase adj locked adj loop) or pll)) with ((second adj ((phase adj locked adj loop) or pll)) with (VCO or (voltage adj controlled adj oscillator))) WITH SERIE and ((mobile adj station) or MS or (base adj station) OR CDMA)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:46
L71	0	("2005/0062547").URPN.	USPAT	OR	ON	2007/01/23 20:46
L72	2	"20060085662".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:46
L73	2	"5875186".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:46
L74	1	(first adj ((phase adj locked adj loop) or pll)) with ((second adj ((phase adj locked adj loop) or pll)) and (VCO or (voltage adj controlled adj oscillator))) and (wlan)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:46
L75	2	"6594508".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:46

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L76	2	"6181923".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:46
L77	2	(first adj ((phase adj locked adj loop) or pll)) same ((second adj ((phase adj locked adj loop) or pll)) and (VCO or (voltage adj controlled adj oscillator)))) and (wlan)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:46
L78	41	44 and 53	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:53
L79	11	44 and 56	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/01/23 20:50

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wo99/08456: 1 record

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Refine Search

wo99/08456



Title	Pub. Date	Int. Class	Applicant
1. (WO 1999/008456) COMMUNICATION SYSTEM UTILIZING HOST SIGNAL PROCESSING	18.02.1999	H04B 1/38	COMSYS COMMUNICATION & SIGNAL PROCESSING LTD.

A communications system utilizing host signal processing techniques particularly applicable to cellular communication system devices that are integrated with a system that incorporates a general purpose CPU running a multitasking operating system, e.g., a portable or handheld computer. The cellular communication system includes a cellular modem, cellular control/protocol function and an RF module (234). Additional components include a voice codec, analog modem and optional speaker phone. Conventional cellular communication systems typically utilize a dedicated DSP processor, a controller, memory devices and analog circuitry to implement cellular system functionality. Some of the processing tasks that are adapted to execute on the host CPU (...)

Search Summary



WO99/08456: 1 occurrence in 1 record.

Search Time: 0.04 seconds.





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Antenna and cable monitoring for radio base station - Patent 6594508

The **second phase locked loop** functions in a similar manner to the **first phase locked loop** described above. Specifically, the cable loss phase detector 636 ...
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Automatic frequency control circuit and method of automatic ...

Hereupon, the first voltage controlled oscillator (VCO) 301 outputs oscillation frequency (f).
The **first phase locked loop** circuit (PLL circuit) 302 ...
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Dynamic wireless local area network with interactive ...

The **first phase-locked loop**, called the low frequency (LF) phase-locked loop 3900, generates a reference signal for the **second phase-locked loop**, ...
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and shift of VCO voltage to region outside linear region. ... **second phase-locked loop** circuit receives the **first phase-locked loop** output ...
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[Radio-Electronics.Com :: PLL Frequency Synthesizer Tutorial](#)

The **second phase locked loop**, PLL, has the divider set to 19, ... In turn this means that the frequency of the **VCO** must operate at 29.9 MHz. ...

www.radio-electronics.com/info/receivers/synth_basics/synth_basics.php - 33k -

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[Phase-locked loop circuitry for programmable logic devices ...](#)

a **second phase-locked loop** circuit configured to respond to the output of the ... the voltage controlled oscillator (**VCO**) circuitry is configured to produce ...

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[Stereo and dual audio signal identifying system - Patent 5432855](#)

a **second phase-locked-loop** locking phase between an externally generated ... and generating an AM-detected output, a **first phase-locked-loop** locking phase ...

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The **first phase locked loop** synchronizes the. frequency of **VCO** and the line.

synchronization pulses from the ... comparator of the **second phase locked loop** ...

ieeexplore.ieee.org/iel1/30/1683/00044286.pdf?arnumber=44286 - [Similar pages](#)

[CIPO - Canadian Patent Database - Claims - 1257337](#)

... including a first voltage-controlled oscillator (**VCO**) for generating an ... a **second phase-locked loop**, wherein the **first phase-locked loop** includes a ...

patents1.ic.gc.ca/claims?patent_number=1257337&language=X - 16k -

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[Frequency synthesizer - US Patent 4720688](#)

first phase-locked loop means having a first voltage-controlled oscillator ... a **second phase-locked loop** having a second **VCO** st at a variable frequency ...

www.patentstorm.us/patents/4720688-claims.html - 24k - [Cached](#) - [Similar pages](#)

[VCO having voltage-to-current converter and PLL using same - US ...](#)

A phase-locked loop circuit having a **first phase-locked loop** that synchronizes to a data pulse string and a **second phase-locked loop** that synchronizes to a ...

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[United States Patent: 4293825](#)

R. The **second phase locked "loop"** L2 receives the sum frequency $f_{sub.o} + f_{sub.R}$ coming from the **first phase locked "loop"** and a frequency $f_{sub.vco}$ coming ...

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[Superheterodyne tranceiver with bilateral first mixer and dual ...](#)

A **first phase locked loop** circuit is coupled to the first mixer. ... The preferred PLL 38 includes a voltage controlled oscillator 101 (**VCO**) which has an ...

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EP979000 Thomson european software patent - Phase lock loop with ...

The **second phase locked loop**, which for example, operates at the same frequency, ...

[0004] The response of the **first phase locked loop** may be optimized for ...

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"first phase locked loop" AND "second phase locked loop"

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- ☐ 1. [Frequency synthesizer and method of providing a mixing oscillator signal to a mixer](#)
Heymann, Roland, UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT, Aug 2003
...invention the **second phase locked loop 2** is provided...path of the **first phase locked loop 1**, which...point. The **second phase locked loop 2** also includes...oscillator (**VCO 2**) 14 and...includes a **first phase locked loop** downstream of whose **VCO** (voltage...oscillator) a **second phase locked loop** is connected...
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- ☐ 2. [Clock generator for generating internal clock signal synchronized with reference clock signal](#)
Mano, Ryuji / Yoshimura, Tsutomu, UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT, May 2003
...each other. **First phase-locked loop L 11** has the...circuit **O 11** of **first phase-locked loop L 11** has the...FIG. 4, when **first phase-locked loop L 11** has high-speed **VCO** characteristics...state. In **second phase-locked loop L 21**, control...
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- ☐ 3. [Synchronous generating circuit devices with two phase-locked loops and feedback around both](#)
Kurata, Hirotaka, Tokyo, JP, UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT, Jan 1979
...sub.2. The **first phase-locked loop PLL.sub.1** comprises a first **VCO 1**, a first...FIG. 4). The **second phase-locked loop PLL.sub.2**...output of the **VCO** is delayed...again, the **first phase-locked loop PLL.sub. 1**...the first **VCO 1** is stabilized...2 and the **second phase-locked loop** is so arranged...
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- ☐ 4. [CLOCK RECOVERY CIRCUIT](#)

Re
US
foi
arr
car
cor
del
div
err
fre
inp
int
pll
sul
syr
syr
tin
tra
vid
Or
Al
F

KUPFER, Theodor, *PATENT COOPERATION TREATY APPLICATION*, Nov 2002


...holdover state, the **VCO** and the VCXO are locked...digital data signal. The **VCO** follows the VCXO, which...5 data signal, the **VCO** and the VCXO must enter...noise ratio includes a **first phase locked loop** circuit operating 30...the data signal, a **second phase locked loop** circuit for operating...

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- ☐ 5. [METHOD AND APPARATUS FOR REDUCING OSCILLATOR NOISE BY NOISE-FEEDFORWARD](#)

DENT, Paul W., *PATENT COOPERATION TREATY APPLICATION*, Oct 2000


...includes a **first phase- locked loop** circuit 12...14 and a **second phase- locked loop** circuit 16. The **first phase-locked loop** circuit 12...oscillator (**VCO**) 18 which...MHz. The **VCO** 18 of the **first phase-locked loop** 12 is preferably...

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- ☐ 6. [Frequency synthesizer for broadcast telephone system having multiple assignable frequency channels](#)

Paneth, Eric, Givataim, IL, *UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT*, Aug 1989


...frequency. The **first phase- locked loop** 12 includes a first **VCO** 26, a mixer...filter 34. The **second phase- locked loop** 14 includes...includes a **first phase-locked loop** connected to a **second phase-locked loop** for enhancing...resolution. The **first phase-locked loop** includes...oscillator (**VCO**) for generating...

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- ☐ 7. [Frequency synthesizer for broadcast telephone system having multiple assignable frequency channels](#)

Paneth, Eric, *UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT*, Nov 1988

...frequency. The **first phase-locked loop** 12 includes a first **VCO** 26, a mixer...filter 34. The **second phase-locked loop** 14 includes...includes a **first phase-locked loop** connected to a **second phase-locked loop** for enhancing...resolution. The **first phase-locked loop** includes...oscillator (**VCO**) for generating...

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- ☐ 8. [Method and apparatus for reducing oscillator noise by noise- feedforward](#)

Dent, Paul W., Pittsboro, NC, *UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT*, Jul 2000

...includes a **first phase-locked loop** circuit 12...14 and a **second phase-locked loop** circuit 16. The **first phase-locked loop** circuit 12...oscillator (**VCO**) 18 which...between the **first phase- locked loop** circuit...102 and the **second phase-locked loop** circuit...controlling the **VCO** 50. The provision...

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- ☐ 9. [Apparatus and method for controlling a phase-locked loop circuit](#)

Audinot, Pascal / Henwood, Andrew M., *UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT*, Nov 2003

...telephone. A **first phase-locked loop** generates...operation of the **first phase-locked loop** being under...control. A **second phase-locked loop** generates...frequency


of the **first phase-locked loop** and having...frequency of the **second phase-locked loop**. A further...

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☐ **10. Clock recovery for multiple frequency input data**

Fang, Al X., UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT, May 2001


...so that the first **VCO** 314 oscillates at 128...input of the first **VCO**, produces a control...description of FIG. 3, **second phase locked loop** 320 includes a second...oscillator such as a second **VCO** 324. The control signal...signal 316 from the **first phase locked loop** 310 may be regarded...

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☐ **11. Local oscillator circuit having two phase locked loops having respective frequency dividers with a common division ratio**

Kumagai, Tadashi, Soma, JP, UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT, Sep 1980


...11 and comprises a **first phase locked loop** 12 and a **second phase locked loop** 13. The **first phase locked loop** 12 comprises a voltage...controlled oscillator (**VCO**) 14 which produces...of the **VCO** 14. The **second phase locked loop** 13 comprises a voltage...

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☐ **12. FREQUENCY SYNTHESIZER**

HORIE, HIROSHI, PATENT ABSTRACTS OF JAPAN, Oct 1988


...frequency of the **VCO** and a reference...CONSTITUTION: A **first phase locked loop** consists...while a **second phase locked loop** includes...filter 3, a **VCO** 4, and a...adjusted by the **first phase locked loop** so that the...frequency of the **VCO** 4 is controlled by the **second phase locked loop**. As a result...

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☐ **13. Low noise fine frequency step synthesizer**

Yang, Steve S. / Arnold, Keith P., EUROPEAN PATENT, Jun 1993

...entitled "**VCO** Controlled...includes a **first phase locked loop** comprising...detector. A **second phase locked loop** having a...reference. The **first phase locked loop** 12 is coupled...of the VHF **VCO** 21. The video...output of the **first phase locked loop** 12 is coupled into the **second phase locked loop** 13 by a third...

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☐ **14. LOW JITTER PHASE-LOCKED LOOP WITH DUTY-CYCLE CONTROL**


O'BRIEN, David E. / SHEEN, Timothy W. / HUTNER, Marc R. / MITTELBRUNN, Michael A. / SABIL, Abdelkebir, PATENT COOPERATION TREATY APPLICATION, Apr 2001


...includes a **first phase-locked loop** that provides...signal, and a **second phase-locked loop** that provides...coupled to the **first phase-locked loop** and an inverted...coupled to the **second phase-locked loop**. In accordance...generating, by the **first phase-locked loop**, a first...


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- ☐ **15. [Television synchronizing signal reproducing apparatus](#)**
Munezawa, Kazushi, Tokyo, JP / Tsuru, Tashihiko, Tokyo, JP, UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT, Aug 1984
...composite video signal; a **first phase- locked loop** circuit for producing a first...horizontal synchronizing signal; a **second phase-locked loop** circuit for producing a second...voltage controlled oscillator (**VCO**) responsive to the output...dividing the output of said **VCO** to provide said first signal...
Full text available at patent office. For more in-depth searching go to  LexisNexis
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- ☐ **16. [METHOD AND APPARATUS FOR VERTICALLY LOCKING INPUT AND OUTPUT VIDEO SIGNALS](#)**
TARACI, Brian, Richard / TROUNG, Duy, Duc, PATENT COOPERATION TREATY APPLICATION, Mar 2002
This invention describes a method and apparatus for vertically locking input and output video frame rates. The output vertical sync pulse is locked in phase with the input vertical sync pulse, regardless of the input format and frequency. The output ...
Full text available at patent office. For more in-depth searching go to  LexisNexis
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- ☐ **17. [Low jitter phase-locked loop with duty-cycle control](#)**
O'Brien, David E. / Sheen, Timothy W. / Hutner, Marc R. / Mittelbrunn, Michael A. / Sabil, Abdelkebir, UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT, Mar 2002
...feedback of the PLL 712 / 714 , and the **VCO** 916 converts a voltage from the loop filter...each divide the output frequency of the **VCO** by a predefined constant. The PGA amplifies...the PLL and has the effect of dividing the **VCO** frequency by a constant "N. "
The second...
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- ☐ **18. [Frequency synthesizer](#)**
Yabuki, Hiroyuki / Makimoto, Mitsuo, UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT, Jul 1994
...frequency of the **second phase- locked loop** circuit 16...that of the **first phase-locked loop** circuit 9...frequency of the **second phase-locked loop** circuit 16...that of the **first phase- locked loop** circuit 9...that the **second phase-locked loop** circuit 16...
Full text available at patent office. For more in-depth searching go to  LexisNexis
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- ☐ **19. [Frequency synthesizer](#)**
Yabuki, Hiroyuki / Makimoto, Mitsuo, EUROPEAN PATENT, Sep 1993
...output of the **second phase-locked loop** circuit. After...switched to the **first phase-locked loop** circuit, the...gain of the **second phase-locked loop** circuit is...that of the **first phase-locked loop** circuit. Furthermore...that of the **first phase-locked loop** circuit 9...preferable that the **second phase-locked loop** circuit 16...
Full text available at patent office. For more in-depth searching go to  LexisNexis
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- ☐ **20. [Lock detector for a dual phase locked loop system](#)**
Fernandez-TeXon, Francisco, UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT, Jun 2002

...locked condition. Master PLL 12 produces a **VCO** clock signal 24 which, when frequency divided...22. Similarly, slave PLL 14 produces a **VCO** clock signal 36 which, when frequency divided...lead or lag a predetermined number of its **VCO** clock cycles within a predetermined number...

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- ☐ 1. Antenna and cable monitoring for radio base station
Ketonen, Veli-Pekka, UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT, Jul 2003
...station 104 to which the **mobile station** 110 is coupled by way...108 formed between the **mobile station** 110 and the radio base...signals (signals from a **mobile station** to the base station...oscillator (VCTCXO or **VCO**) 410 . A VCTCXO outputs...
Full text available at patent office. For more in-depth searching go to LexisNexis
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- ☐ 2. Automatic frequency control circuit and method of automatic frequency control
Kawano, Osamu / Inagami, Fujio, UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT, Jan 2001
...from the **mobile station** control unit...oscillator (**VCO**) 301 outputs...f). The **first phase locked loop** circuit...from the **mobile station** control unit...oscillator (**VCO**) 303 outputs...301. The **second phase locked loop** circuit...
Full text available at patent office. For more in-depth searching go to LexisNexis
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- ☐ 3. VIRTUAL CARRIER DETECTION FOR WIRELESS LOCAL AREA NETWORK WITH DISTRIBUTED CONTROL
BIBA, Kenneth J. / BELANGER, Philip H. / BAUGH, William N. / ROSEN, David B. / CRIPPS, Peter K., PATENT COOPERATION TREATY APPLICATION, Jan 1995
A wireless network has a distributed control protocol using carrier sense mutiple access. Each station in the network listens to traffic on the network communications channel (typically frequency hopping radio transmissions using spread spectrum). Based ...
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☐ 1. RECEIVER, ESPECIALLY FOR MOBILE RADIO COMMUNICATION

BOOS, Zdravko, *EUROPEAN PATENT*, Apr 2003

...ist ein als PLL-Regelkreis ausgeführter **VCO** gezeigt, der über einen (n:m)-Frequenzvervielfacher...Codevielfachzugriff (Code Division Multiple Access, **CDMA**) unterstützt werden. In dem den zweiten...T, einen spannungsgeregelten Oszillator **VCO** sowie ein Schleifenfilter LF. Ebenso wie...

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☐ 2. VERY LOW NOISE LOCAL OSCILLATOR FOR USE IN WIRELESS COMMUNICATION TRANSCEIVER

KEREN, Yossi, *PATENT COOPERATION TREATY APPLICATION*, Jun 2002

...Multiple Access (**CDMA**), Time Division...comprises a **first phase locked loop**, a frequency...mixer. The **first phase locked loop** comprises...signal. The **second phase locked loop** comprises...signal from **first phase locked loop** and to control...

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☐ 1. METHOD FOR CLOCK SYNCHRONIZATION OF WIRELESS 1394 BUSES FOR NODES CONNECTED VIA IEEE 802.11 LAN

BENNETT, Jeff, *PATENT COOPERATION TREATY APPLICATION*, Dec 2004

...the master to a **second PLL**. This use of a **second PLL** allows for error...to that of the **first PLL** 225 of the master...communication 214 with **WLAN** devices 213...Alert 216.

The **first PLL** 225 is preferably...master to the **second PLL** 235. The **second**...

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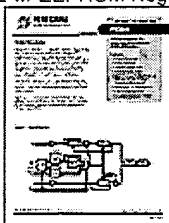
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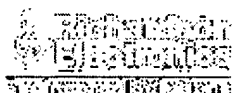
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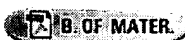
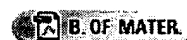
The FlexiPower prescalers are supplied power on dedicated pins and can operate at a substantial power savings at voltages as low as 0.8 volts, while allowing a 3 volt charge pump supply. For 3 volt only systems, on-chip voltage regulation may be used to generate the prescaler power supplies.

The prescaler power supply may be provided externally or internally regulated down from V_{dd}. In a typical 950 MHz application the total current consumed by the PLL is 2.1 mA. Operation at reduced current levels provides significant battery life extension. The PE3291 allows the system designer to minimize power consumption by controlling the voltage on the prescaler.

PE3291 provides fractional-N division with power-of-two denominator values up to 32. This allows comparison frequencies up to 32 times the channel spacing, providing a lower phase noise floor than integer PLLs. The 32/33 RF prescaler (PLL1) operates up to 1.2 GHz and the 16/17 IF prescaler (PLL2) operates up to 550 MHz.

**Application Notes**

- **AN3** - Using the PE3291 in Narrow Band/Paging Applications
- **AN4** - Using the PE3291/92 in CDMA Applications
- **AN5** - Using the PE329x Series Fractional-N PLL's
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